From the INTERNATIONAL BUREAU

PCT

NOTIFICATION CONCERNING TRANSMITTAL OF COPY OF INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY (CHAPTER I OF THE PATENT COOPERATION TREATY)
(PCT Rule 44bis.1(c))

To:

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ETATS-UNIS D'AMERIQUE

Date of mailing *(day/month/year)*	
18 December 2008 (18.12.2008)	
Applicant's or agent's file reference	IMPORTANT NOTICE
0057-014P1PCT	

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US2007/004030	16 February 2007 (16.02.2007)	16 February 2006 (16.02.2006)

Applicant
VNS PORTFOLIO LLC et al

The International Bureau transmits herewith a copy of the international preliminary report on patentability (Chapter I of the Patent Cooperation Treaty)

The International Bureau of WIPO	Authorized officer
34, chemin des Colombettes 1211 Geneva 20, Switzerland	Yolaine Cussac

PATENT COOPERATION TREATY

PCT

INTERNATIONAL PRELIMINARY REPORT ON PATENTABILITY
(Chapter I of the Patent Cooperation Treaty)

(PCT Rule 44*bis*)

Applicant's or agent's file reference 0057-014P1PCT	**FOR FURTHER ACTION**	See item 4 below
International application No. PCT/US2007/004030	International filing date *(day/month/year)* 16 February 2007 (16.02.2007)	Priority date *(day/month/year)* 16 February 2006 (16.02.2006)
International Patent Classification (8th edition unless older edition indicated) See relevant information in Form PCT/ISA/237		
Applicant VNS PORTFOLIO LLC		

1. This international preliminary report on patentability (Chapter I) is issued by the International Bureau on behalf of the International Searching Authority under Rule 44 *bis*.1(a).

2. This REPORT consists of a total of 6 sheets, including this cover sheet.

   In the attached sheets, any reference to the written opinion of the International Searching Authority should be read as a reference to the international preliminary report on patentability (Chapter I) instead.

3. This report contains indications relating to the following items:

☒	Box No. I	Basis of the report
☐	Box No. II	Priority
☐	Box No. III	Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
☐	Box No. IV	Lack of unity of invention
☒	Box No. V	Reasoned statement under Article 35(2) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
☐	Box No. VI	Certain documents cited
☐	Box No. VII	Certain defects in the international application
☐	Box No. VIII	Certain observations on the international application

4. The International Bureau will communicate this report to designated Offices in accordance with Rules 44*bis*.3(c) and 93*bis*.1 but not, except where the applicant makes an express request under Article 23(2), before the expiration of 30 months from the priority date (Rule 44*bis* .2).

	Date of issuance of this report 03 December 2008 (03.12.2008)
The International Bureau of WIPO 34, chemin des Colombettes 1211 Geneva 20, Switzerland	Authorized officer Yolaine Cussac
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PATENT COOPERATION TREATY

From the
INTERNATIONAL SEARCHING AUTHORITY

To:
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WRITTEN OPINION OF THE
INTERNATIONAL SEARCHING AUTHORITY

(PCT Rule 43*bis*.1)

Date of mailing *(day/month/year)*	10 NOV 2008

Applicant's or agent's file reference	FOR FURTHER ACTION
0057-014P1P	See paragraph 2 below

International application No.	International filing date *(day/month/year)*	Priority date *(day/month/year)*
PCT/US 07/04030	16 February 2007 (16.02.2007)	16 February 2006 (16.02.2006)

International Patent Classification (IPC) or both national classification and IPC
IPC(8) - G06F 15/00 (2008.04)
USPC - 712/221

Applicant TECHNOLOGY PROPERTIES LIMITED

1. This opinion contains indications relating to the following items:

- ☒ Box No. I Basis of the opinion
- ☐ Box No. II Priority
- ☐ Box No. III Non-establishment of opinion with regard to novelty, inventive step and industrial applicability
- ☐ Box No. IV Lack of unity of invention
- ☒ Box No. V Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement
- ☐ Box No. VI Certain documents cited
- ☐ Box No. VII Certain defects in the international application
- ☐ Box No. VIII Certain observations on the international application

2. FURTHER ACTION

If a demand for international preliminary examination is made, this opinion will be considered to be a written opinion of the International Preliminary Examining Authority ("IPEA") except that this does not apply where the applicant chooses an Authority other than this one to be the IPEA and the chosen IPEA has notified the International Bureau under Rule 66.1*bis*(b) that written opinions of this International Searching Authority will not be so considered.

If this opinion is, as provided above, considered to be a written opinion of the IPEA, the applicant is invited to submit to the IPEA a written reply together, where appropriate, with amendments, before the expiration of 3 months from the date of mailing of Form PCT/ISA/220 or before the expiration of 22 months from the priority date, whichever expires later.

For further options, see Form PCT/ISA/220.

3. For further details, see notes to Form PCT/ISA/220.

Name and mailing address of the ISA/US	Date of completion of this opinion	Authorized officer:
Mail Stop PCT, Attn: ISA/US Commissioner for Patents P.O. Box 1450, Alexandria, Virginia 22313-1450 Facsimile No. 571-273-3201	31 October 2008 (31.10.2008)	Lee W. Young PCT Helpdesk: 571-272-4300 PCT OSP: 571-272-7774

Form PCT/ISA/237 (cover sheet) (April 2007)

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
PCT/US 07/04030

Box No. 1 Basis of this opinion

1. With regard to the **language**, this opinion has been established on the basis of:

   ☒ the international application in the language in which it was filed.

   ☐ a translation of the international application into _____ which is the language of a translation furnished for the purposes of international search (Rules 12.3(a) and 23.1(b)).

2. ☐ This opinion has been established taking into account the **rectification of an obvious mistake** authorized by or notified to this Authority under **Rule 91** (Rule 43*bis*.1(a))

3. With regard to any **nucleotide and/or amino acid sequence** disclosed in the international application, this opinion has been established on the basis of:

   a. type of material

      ☐ a sequence listing

      ☐ table(s) related to the sequence listing

   b. format of material

      ☐ on paper

      ☐ in electronic form

   c. time of filing/furnishing

      ☐ contained in the international application as filed

      ☐ filed together with the international application in electronic form

      ☐ furnished subsequently to this Authority for the purposes of search

4. ☐ In addition, in the case that more than one version or copy of a sequence listing and/or table(s) relating thereto has been filed or furnished, the required statements that the information in the subsequent or additional copies is identical to that in the application as filed or does not go beyond the application as filed, as appropriate, were furnished.

5. Additional comments:

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.
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Box No. V **Reasoned statement under Rule 43*bis*.1(a)(i) with regard to novelty, inventive step or industrial applicability; citations and explanations supporting such statement**

1. Statement

Novelty (N)	Claims	5, 9, 11, 12, 15-21	YES
	Claims	1-4, 6-8, 10, 13, 14	NO
Inventive step (IS)	Claims	None	YES
	Claims	1-21	NO
Industrial applicability (IA)	Claims	1-21	YES
	Claims	None	NO

2. Citations and explanations:

Claims 1-4, 6-8, 10, 13 and 14 lack novelty under PCT Article 33(2) as being anticipated by US 6,233,670 B1 to Ikenaga et al. (hereinafter 'Ikenaga').

Regarding claim 1, Ikenaga discloses in a computer for executing a series of instructions (Figs 1, 7; col 4, ln 52-54), an improvement comprising: an instruction register for temporarily storing a group of instructions to be executed (Fig 1 and col 4, ln 44-47 -- e.g., one of improved function units 4, 5, 6, and 7); and a program counter for storing an address from which a group of instructions is retrieved into said instruction register (Figs 1, 7; col 1, ln 42-44; col 4, ln 52-54); wherein the address in said program counter can be either a memory address or the address of a register (col 1, ln 42-44 -- e.g., a memory address to instruction memory 1).

Regarding claim 2, Ikenaga further discloses wherein: the address in said program counter can, optionally, point to a plurality of registers (Figs 1, 8C and col 6, ln 59-65 -- e.g., to function units 4 and 5).

Regarding claim 3, Ikenaga further discloses wherein: said group of instructions includes more than one instruction (Fig 8C and col 6, ln 59-65 -- e.g., instructions 11 and 12).

Regarding claim 4, Ikenaga further discloses wherein: when there are no instructions left to be executed in the instruction register then the computer will fetch an instruction group according to the address stored in the program counter (Fig 8C and col 1, ln 42-44 -- e.g., when instructions 11 and 12 have both been fully executed, fetching another instruction group based on the address signal generated from the program counter).

Regarding claim 6, Ikenaga further discloses wherein: when an instruction in said group of instructions is a jump instruction (Fig 8C and col 7, ln 7-23 -- bypass), then the program counter is loaded with an address indicated by the jump instruction (col 7, ln 7-23).

Regarding claim 7, Ikenaga further discloses wherein: the address indicated by the jump instruction follows the jump instruction in the group of instructions (Figs 1, 8C; col 6, ln 63-65 and col 7, ln 7-23 -- e.g., the address and the instruction associated with function units that follow each other such as function units 4 and 5).

Regarding claim 8, Ikenaga discloses a method for executing instructions in a computer, (Figs 1, 7; col 4, ln 52-54) comprising: (a) fetching a group of instructions from an address (Fig 1 and col 4, ln 44-47 -- instruction fetching stage 2), wherein the address can be either an address of a memory location or an address of a port (col 1, ln 42-44 -- e.g., a memory address to instruction memory 1); (b) placing said group of instructions in an instruction register to be executed (Fig 1 and col 4, ln 44-54 -- e.g., placing in one of improved function units 4, 5, 6, and 7); and (c) executing at least one of said group of instructions from said instruction register (Fig 8C and col 6, ln 51-64).

Regarding claim 10, Ikenaga further discloses wherein: when all of the instructions in the instruction group have been executed then yet another group of instructions is fetched (Fig 8C and col 1, ln 42-44 -- e.g., when instructions 11 and 12 have both been fully executed, fetching another instruction group based on the address signal generated from the program counter).

Regarding claim 13, Ikenaga further discloses: in step (c) either executing all instructions in said group of instructions or else executing the instructions in said group of instructions until a diversion instruction is encountered (Fig 8C and col 7, ln 7-23 -- e.g., executing until a bypass occurs); wherein said diversion instruction is an instruction that provides for fetching a group of instructions from yet another location (col 6, ln 63-65 and col 7, ln 7-23 -- e.g., data executed in the other pipeline PL1 is applied; Fig 2 and col col 6, ln 51-57 -- fetching stage 2).

Regarding claim 14, Ikenaga further discloses wherein: the diversion instruction is a JUMP instruction (Fig 8C and col 7, ln 7-23 -- bypass).

-- See Supplemental Box --

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

International application No.

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.
Continuation of:
Box No. V.2. Citations and explanations:

Claims 5, 11, 12 and 21 lack an inventive step under PCT Article 33(3) as being obvious over Ikenaga in view of US 5,434,989 A (Yamaguchi).

Regarding claim 5, Ikenaga teaches the computer of claim 1 and further discloses that: when the computer retrieves a group of instructions from a memory, then the program counter is incremented (Fig 8C; col 1, ln 42-44 and col 5, ln 7-9 -- e.g., when instructions 11 and 12 have both been fully executed, another group of instruction is retrieved based on the address signal generated from the program counter such as from source addresses SA1 and SA2). Ikenaga does not expressly discloses that: when the computer retrieves a group of instructions from a register, then the program counter is not incremented. However, Yamaguchi does teach that: when the computer retrieves a group of instructions from a register, then the program counter is not incremented (col 3, ln 48 to col 4, ln 11 -- e.g., by utilizing an address type of a third or fourth type said types not associated with incrementing the program counter). It would have been obvious to one of ordinary skill in the art to modify the computer of Ikenaga so as to not increment the program counter as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from computers configured to not increment the address if the address is that of a port, because such computers can be implemented using multiple types of address types, thereby increasing the flexibility of the design to the particular application of interest to the designer (Yamaguchi col 3, ln 48 to col 4, ln 11).

Regarding claim 11, Ikenaga teaches the method of claim 10 and further discloses that if the address is the address of a memory location, then the address is incremented before the yet another group of instructions is fetched (Fig 8C; col 1, ln 42-44 and col 5, ln 7-9 -- e.g., when instructions 11 and 12 have both been fully executed, fetching another instruction group based on the address signal generated from the program counter such as from source addresses SA1 and SA2). Ikenaga does not expressly disclose that if the address is the address of a port, then the address is not incremented before the yet another group of instructions is fetched. However, Yamaguchi does teach that if the address is the address of a port, then the address is not incremented before the yet another group of instructions is fetched (col 3, ln 48 to col 4, ln 11 -- e.g., by utilizing an address type of a third or fourth type said types not associated with incrementing the program counter). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to not increment the address before fetching another group of instructions if the address is that of a port as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from methods that do not increment the address if the address is that of a port, because such methods can be implemented using multiple types of address types, thereby increasing the flexibility of the method to the particular application of interest to the designer (Yamaguchi col 3, ln 48 to col 4, ln 11).

Regarding claim 12, Ikenaga teaches the method of claim 8 but does not expressly disclose that the address can indicate more than one port. However, Yamaguchi does teach that the address can indicate more than one port (col 3, ln 13-19). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to utilize an address that can indicate more than one port as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from methods that utilize addresses that can indicate more than one port, because such methods can be used in dual port memory arrays (Yamaguchi col 3, ln 13-19).

Regarding claim 21, Ikenaga discloses a computer for executing a series of instructions (Figs 1, 7; col 4, ln 52-54), the computer comprising: an instruction register for temporarily storing a group of instructions (Fig 1 and col 4, ln 44-47 -- e.g., one of improved function units 4, 5, 6, and 7); a logic unit for executing the instructions stored in said instruction register (Fig 5 and col 6, ln 37-45); and means for fetching the group of instructions into said instruction register (Fig 1 and col 4, ln 44-47 -- instruction fetching stage 2). Ikenaga does not expressly disclose fetching from a port. However, Yamaguchi does teach fetching from a port (col 3, ln 13-19). It would have been obvious to one of ordinary skill in the art to modify the computer of Ikenaga so as to fetch from a port as taught by Yamaguchi, because Ikenaga and Yamaguchi are directed to systems and methods for processing data and instructions in an efficient manner. Furthermore, designers benefit from computers with instructions for fetching from a port, because such computers can incorporate dual port memory arrays (Yamaguchi col 3, ln 13-19).

Claims 9 and 15-20 lack an inventive step under PCT Article 33(3) as being obvious over Ikenaga in view of US 4,868,745 A to Patton et al. (hereinafter 'Patton').

Regarding claim 9, Ikenaga teaches the method of claim 8 but does not expressly discloses that the address is retrieved from a program counter register. However, Patton does teach that the address is retrieved from a program counter register (col 3, ln 51-58 and col 4, ln 6-8 -- e.g., from a prologue in the immobile code area; Fig 6D and col 10, ln 9-14). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to retrieve the address from a program counter register as taught by Patton, because Ikenaga and Patton are directed to systems and methods for executing instructions and processing data with a minimum of processing steps. Furthermore, designers benefit from methods that execute instructions using an address retrieved from a program counter register, because such methods allow for intermixing data, pointers and instructions to be executed directly or indirectly (Patton col 2, ln 6-29).

-- See next Supplemental Box --

WRITTEN OPINION OF THE INTERNATIONAL SEARCHING AUTHORITY

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Supplemental Box

In case the space in any of the preceding boxes is not sufficient.

Continuation of:
Box No. V.2. Citations and explanations:

Regarding claim 15, Ikenaga discloses a method for handling data blocks in a computer (Fig 1, 7; col 4, ln 52-54; Fig 8C and col 6, ln 52-65 -- e.g., data blocks comprising instructions 11 and 12), comprising: (a) fetching a data block from an address (Fig 1 and col 4, ln 44-47 - - instruction fetching stage 2; Fig 8C -- e.g., a data block comprising instruction 11, instruction 12, or both), wherein the address can be either an address of a memory location or an address of a port (col 1, ln 42-44 -- e.g., a memory address to instruction memory 1); and (b) if said data block contains a group of instructions then providing said data block to an instruction register (Fig 8C and col 6, ln 59-65 -- e.g., providing instruction 11 and 12 to function units 4 and 5). Ikenaga further discloses that (c) if said data block contains data then providing said data block to the top of a data stack (Fig 2 and col 5, ln 7-15 -- e.g., data comprising SA1, SA2 and DA). Ikenaga does not expressly disclose that the data block contains data rather than instructions. However, Patton does teach that the data block contains data rather than instructions (Fig 1 and col 3, ln 2-4; col 1, ln 68, col 2, ln 6-10 and col 3, ln 24-25 -- e.g., objects for direct object execution comprising data but no OPs). It would have been obvious to one of ordinary skill in the art to modify the method of Ikenaga so as to utilize a data block that contains data rather than instructions as taught by Patton, because Ikenaga and Patton are directed to systems and methods for executing instructions and processing data with a minimum of processing steps. Furthermore, designers benefit from methods that process data alone, because such methods allow for direct or indirect execution or processing regardless of the nature of the intermixed data, pointers and instructions (Patton col 2, ln 6-29).

Regarding claim 16, Ikenaga and Patton teach the method of claim 15. Ikenaga further discloses wherein: said group of instructions can, optionally, also contain data (col 5, ln 7-9).

Regarding claim 17, Ikenaga and Patton teach the method of claim 15. Ikenaga further discloses wherein: the question of whether said data block contains a group of instructions or data is determined by whether the last instruction in a previous group of instructions has been executed (Fig 8C and col 5, ln 7-9 -- e.g., when a previous group comprising instructions 11 and 12 has been executed, decoding stage 3 obtains a new instruction comprising first an instruction code OP; col 7, ln 14-23 -- e.g., and when instructions 11 and 12 have not yet been fully executed, data is transmitted through bypass line 12).

Regarding claim 18, Ikenaga and Patton teach the method of claim 17. Ikenaga further discloses wherein: when the last instruction in said previous group of instructions has been executed then it is determined that the data block contains a group of instructions (Fig 8C and col 5, ln 7-9 -- e.g., when a previous group comprising instructions 11 and 12 has been executed, decoding stage 3 obtains a new instruction that includes an instruction code OP).

Regarding claim 19, Ikenaga and Patton teach the method of claim 15. Patton further discloses wherein: the data stack is a primary data stack (Fig 6A -- P4, PS; Fig 5 and col 3, ln 6-23 and col 5, ln 65-66-- e.g., primary and sole data stack in the data processing system of Fig 5).

Regarding claim 20, Ikenaga and Patton teach the method of claim 15. Ikenaga further discloses that if said data block contains a group of instructions, then executing instructions from said group of instructions from the instruction register (Fig 8C and col 6, ln 51-65).

Claims 1-21 have industrial applicability as defined by PCT Article 33(4) because the subject matter can be made or used in industry.